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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional)
		SCS-550-476
	Application Number	Filed
	10/714,484	November 17, 2003
	First Named Inventor	
	WATT	
	Art Unit	Examiner
	2194	A. Seye
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.</p> <p>I am the <input type="checkbox"/> Applicant/Inventor <input type="checkbox"/> Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96) <input checked="" type="checkbox"/> Attorney or agent of record 27,393 (Reg. No.) <input type="checkbox"/> Attorney or agent acting under 37CFR 1.34. Registration number if acting under 37 C.F.R. § 1.34 _____</p> <p>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*</p> <p><input checked="" type="checkbox"/> *Total of 1 form/s are submitted.</p>		

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**STATEMENT OF ARGUMENTS IN SUPPORT OF**  
**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

The following listing of clear errors in the Examiner's rejection and his failure to identify essential elements necessary for a *prima facie* basis of rejection is responsive to the Final Official Action mailed November 27, 2007 and the Advisory Action faxed on March 27, 2008. The comments in the Request for Reconsideration filed on February 27, 2008 are incorporated by reference.

**Error #1. The Examiner errs in suggesting that Saito Figure 5 element 123 and paragraph 82 contain any disclosure of Applicants' claimed "as commanded by said stub intercept handling routine, suspending execution . . ." step**

On page 4, lines 1-3, the Examiner alleges that the third step of Applicants' independent claim 1 (beginning "as commanded by said stub interrupt handling routine, . . .") is somehow disclosed in Saito's Figure 5 by element 123 as discussed in paragraph 82. The error of this position is clearly set out in the Request for Reconsideration and in the Advisory Action, the Examiner changes his position alleging that Saito's interrupt handler 152 is the claimed "stub interrupt handling routine" and that the interrupt handler 153 is the claimed "main interrupt handling routine."

Assuming that the Examiner construes Saito's business-use OS 110 is the equivalent to the claimed first operating system and the real-time OS 111 is the equivalent to the claimed second operating system, the language of claims 1 and 7 with the Examiner's construction included in brackets, would read as follows:

as commanded by said stub interrupt handling routine [interrupt handler 152 of Saito], suspending execution of said stub interrupt handling routine [152] and starting a main interrupt handling routine interrupt [handler 153 of Saito] executing under control of said second operating system [real-time OS 111 of Saito];

The Examiner's new construction fails to indicate where or how the interrupt handler 152 of Saito's business-use OS 110 suspends itself and starts the interrupt handler 153 of the real-time OS 111 as required by claims 1 and 7. Any reasonable reading of the cited paragraphs 104-105 of Saito provide no teaching of the above claim language.

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Accordingly, the Examiner clearly fails to meet his burden of establishing a *prima facie* case of anticipation because this claimed method step (or the corresponding apparatus elements in independent apparatus claim 7) is not disclosed in Saito. Should the Examiner believe otherwise, he is respectfully requested to specifically identify any teaching in Saito which he contends corresponds to Applicants' claim 1, third step (or the corresponding structure in claim 7). Absent any specific teaching, the Examiner's anticipation rejection of claims 1 and 7 respectfully traversed.

**Error #2. The Examiner repeatedly errs in citing paragraph 63 of Saito as allegedly teaching portions of claim 1 (see paragraphs 2, 3 and 4 on page 4 of the Official Action)**

In paragraphs 2-4 on page 4 of the Final Rejection, the Examiner contends that Saito's paragraph 63 and Figure 6 disclose the subject matter as set out in Applicants' independent claim 1, paragraphs 4, 5 and 6 (and the corresponding paragraphs in independent claim 7). Again, the error of the Examiner's position is clearly obvious by reviewing paragraph 63 of the Saito reference. There is no disclosure of "executing" a main interrupt handling routine or "resuming execution of said stub interrupt handling routine" or "resuming said data processing operations" as specified in independent claim 1, paragraphs 4, 5 and 6 (and the corresponding elements in claim 7).

The Examiner's attention is directed towards the case of *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick*, 221 USPQ 481, 485 (Fed. Cir. 1984) in which the Court of Appeals for the Federal Circuit held that "[a]nticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim."

The Advisory action does not appear to supplement the Final Rejection regarding this claim limitation. Thus, because of the errors noted above and in the Request for Reconsideration, the Final Rejection does not establish any *prima facie* case of "anticipation" because the Rejection fails to identify where any single prior art document teaches each and every method step and each and every claimed interrelationship between method steps as required by Applicants' independent claim 1 or the

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apparatus elements and the interrelationship between the apparatus elements as set out in independent claim 7. Accordingly, claims 1 and 7 and claims dependent thereon are clearly patentable over the Saito reference because of the Examiner's failure to meet his burden of establishing that Saito teaches the claimed steps and elements.

**Error #3. The Examiner again reiterates that he believes that Saito teaches the claimed step of "suspending execution of said stub interrupt handling program and starting a main interrupt handling routine executing under control of said second operating system"**

As noted previously in the Request for Reconsideration, the Examiner goes off on a tangent in terms of support for an "anticipation" rejection that simply has no basis in §102. The Examiner compares **unclaimed** structures of Applicants' preferred embodiment of the claimed invention and various aspects of the Saito document. Importantly, the Examiner's comparison involves **unclaimed subject matter**, i.e., "priority" and possible interrupt handling system priority, and fails to identify any teaching in Saito of the **claimed** subject matter. Whether or not Saito teaches "priority" or "interrupt priority" is irrelevant because this is not claimed in claims 1 and 7.

Again, it would appear that the Examiner is attempting to use any perceived similarity (as opposed to the claimed steps and elements) between the present invention and the prior art as a basis for rejection. As noted previously, the Examiner's reliance upon unclaimed similarities between Saito and the claimed invention involving "priority" or "interrupt priority" is misguided at best.

**Error #4. On page 7, section 9, subsection a, the Examiner erroneously relies upon Saito's paragraphs 63 and 140**

In section 9a on page 7, the Examiner references Saito's priority translation modules 122 and 123 in paragraph 63 and priority reverse translation tables 282 and 283 in paragraph 140 as allegedly disclosing "priorities." However, Applicants' independent claims 1 and 7 do not claim "priority," "priority translation modules" or "priority reverse translation tables." As a result, even assuming that the Saito reference does teach the "priority" related steps and structures, paragraphs 63 nor 140 are not

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even alleged to teach the limitations of Applicants' independent claims 1 and 7 and therefore any further rejection based thereon is respectfully traversed.

**Error #5. The Examiner misinterprets Saito's paragraph 85 which clearly fails to teach a "stub interrupt handling routine" and/or a "starting a main interrupt handling routine"**

The Examiner's reference to Saito's paragraph 85 and Figure 6 in his discussion on page 7 of the Final Rejection is taken as a suggestion that this paragraph contains some teaching of Applicants' claimed subject matter. Again, Applicants can find no disclosure in Saito's Figure 6 or paragraph 85 which discloses claim 1's third step, i.e., "suspending execution of said stub interrupt handling routine and starting a main interrupt handling routine executing under control of said second operating system."

Should the Examiner contend that this is disclosed in some portion of Saito, he is again respectfully requested to identify exactly what language exists in Saito and how he believes this language anticipates the claim language, i.e., "suspending execution . . ." for independent claims 1 and 7. Absent any specific reference, it is clear that the Examiner has failed to meet the burden of establishing anticipation under 35 USC §102.

**Error #6. The Examiner, in his Response to Arguments, erroneously suggests that there is some correspondence between a "priority translation module" in Saito and the claimed "stub interrupt handling routine" recited in Applicants' independent claims 1 and 7**

The Examiner appears to try to justify his discussion of "priority translation module" and "priority translation table" as being associated with "an operating system." The Examiner then appears to suggest that because these priority related modules are associated with an operating system, they somehow disclose Applicants' claimed method of processing data with execution of data processing operations under control of either a first operating system or a second operating system.

In the Saito system, the operating system that runs is set by task priority (see Saito paragraph 108). The operating system of Saito on which the interrupt is run is set by the common interrupt

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handler (see Saito paragraph 105). Saito neither discloses nor suggests that an interrupt under one operating system (e.g., handler 152 of Figure 10 in Saito) starts an interrupt under the other operating system (handler 153 of Figure 10).

Again, the Examiner is challenged to identify specifically where the claimed method steps and apparatus elements are disclosed in Saito. Absent any corresponding disclosure of claimed method steps and apparatus elements in Saito, there is simply no basis for any further rejection under 35 USC §102.

**Error #7. The Examiner appears to misunderstand his burden of proving anticipation and/or obviousness**

Towards the end of paragraph 9a on page 7 of the Final Rejection and in the "Continuation of 11" portion of the Advisory Action, the Examiner asserts that "Although the specified citations are representative of the teachings in the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well." This general allegation does not meet the Federal circuit's required burden of proof as clearly stated in the Request for Reconsideration.

Because the Examiner has failed to demonstrate where any one of the references teach the method steps of claim 1 or the apparatus elements of independent claim 7 or claims dependent thereon, there can be no *prima facie* case of anticipation or obviousness.

There has been no allegation that either Saito or Worley disclose the claimed features of Applicants' independent claims or claims dependent thereon. It is the Examiner's burden to establish a *prima facie* case and, if he cannot do so, the rejections under 35 USC §102 and §103 fail.

In view of the above discussions and those in the Request for Reconsideration, there is no basis for rejection of claims 1 and 7 and claims dependent thereon under 35 USC §102 or §103, as the Examiner has completely failed to establish any *prima facie* case.